# ANNA UNIVERSITY TIRUCHIRAPPALLI
## Tiruchirappalli – 620 024
### Regulations 2008
#### Curriculum

## M.E. VLSI DESIGN

### SEMESTER I

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<th>S.No.</th>
<th>Subject Code</th>
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<th>L</th>
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<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>MA 5131</td>
<td>Applied Mathematics for Electronics Engineers</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>VL5101</td>
<td>Digital Signal Processing Integrated Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>AN5102</td>
<td>Advanced Digital System Design</td>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>AN5103</td>
<td>VLSI Design Techniques</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>VL5102</td>
<td>Solid State Device Modeling and Simulation</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>E1****</td>
<td>Elective I</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Practical</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>VL5103</td>
<td>VLSI Design Laboratory I</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td>23</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SEMESTER II

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>AN 5151</td>
<td>Analysis and Design of Analog Integrated Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>VL 5151</td>
<td>Computer Aided Design of VLSI Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>AN 5152</td>
<td>Computer Architecture and Parallel Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>AN 5154</td>
<td>Embedded Systems</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>E2****</td>
<td>Elective II</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>E3****</td>
<td>Elective III</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td>21</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Practical</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>VL 5152</td>
<td>VLSI Design Laboratory II</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Total</strong></td>
<td>21</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SEMESTER III

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>E4****</td>
<td>Elective IV</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>E5****</td>
<td>Elective V</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>E6****</td>
<td>Elective VI</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

Practical

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>VL5251</td>
<td>Project Work Phase I</td>
<td>0</td>
<td>0</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total</td>
<td></td>
<td></td>
<td></td>
<td>15</td>
</tr>
</tbody>
</table>

Total Credits to be Earned for the Award of the Degree = 71

SEMESTER IV

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Practical</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VL5251</td>
<td>Project Work Phase II</td>
<td>0</td>
<td>0</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Total</td>
<td></td>
<td></td>
<td></td>
<td>12</td>
</tr>
</tbody>
</table>

LIST OF ELECTIVES

<table>
<thead>
<tr>
<th>S.No.</th>
<th>Subject Code</th>
<th>Subject</th>
<th>L</th>
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<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
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<td></td>
</tr>
<tr>
<td>Theory</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>VL5001</td>
<td>Testing of VLSI Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>VL5002</td>
<td>Low Power VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>VL5003</td>
<td>VLSI Signal Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>VL5004</td>
<td>CMOS VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>VL5005</td>
<td>Analog VLSI Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>VL5006</td>
<td>Design of Semiconductor Memories</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>7</td>
<td>VL5007</td>
<td>VLSI Technology</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>VL5008</td>
<td>Physical Design of VLSI Circuits</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>9</td>
<td>VL5009</td>
<td>Genetic Algorithms and their Applications</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>10</td>
<td>AN5104</td>
<td>Advanced Microprocessors and Microcontrollers</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>11</td>
<td>AN5002</td>
<td>Neural Networks and Applications</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>12</td>
<td>AN5005</td>
<td>ASIC Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>13</td>
<td>AN5007</td>
<td>Reliability Engineering</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>14</td>
<td>AN5009</td>
<td>Electromagnetic Interference and Compatibility in System Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>15</td>
<td>CO5006</td>
<td>Speech and Audio Signal Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>16</td>
<td>CO5004</td>
<td>DSP Processor Architecture and Programming</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>17</td>
<td>VL 5025</td>
<td>Special Elective</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>
ANNA UNIVERSITY TIRUCHIRAPPALLI
Tiruchirappalli - 620 024
Regulations 2008

Syllabus

M.E. VLSI DESIGN

SEMESTER I

MA5131 – APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS

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<th>L</th>
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<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
</tbody>
</table>

UNIT I     LINEAR ALGEBRAIC EQUATIONS & EIGEN VALUE PROBLEMS

UNIT II     THE WAVE EQUATIONS

UNIT III    SPECIAL FUNCTIONS
Bessel's Equation – Bessel Functions Legendre's Equation – Legendre Polynomials Rodrigue’s Formula – Recurrence Relations – Generating Functions and Orthogonal Property for Bessel Functions – Legendre Polynomials.

UNIT IV     RANDOM VARIABLES

UNIT V      QUEUING THEORY

L: 45 T: 15 Total: 60

TEXT BOOKS

REFERENCES
UNIT I   DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES   9

UNIT II   DIGITAL SIGNAL PROCESSING   9

UNIT III   DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS   9

UNIT IV   DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES   9
DSP system architectures – Standard DSP architecture – Ideal DSP architectures – Multiprocessors and multicomputers – Systolic and Wave front arrays – Shared memory architectures – Mapping of DSP algorithms onto hardware – Implementation based on complex PEs – Shared memory architecture with Bit-serial PEs

UNIT V   ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN   9
Conventional number system – Redundant Number system – Residue Number System Bit-parallel and Bit-Serial arithmetic – Basic shift accumulator – Reducing the memory size – Complex multipliers – Improved shift-accumulator Layout of VLSI circuits – FFT processor – DCT processor and Interpolator as case studies

TEXT BOOKS

REFERENCES
UNIT I  SEQUENTIAL CIRCUIT DESIGN  9

UNIT II  ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN  9

UNIT III  FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS  9

UNIT IV  SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES  9

UNIT V  SYSTEM DESIGN USING VHDL  9

TEXT BOOKS

REFERENCES
# AN5103 – VLSI DESIGN TECHNIQUES

**L**  | **T**  | **P**  | **C**  
---|---|---|---
3  | 0  | 0  | 3

## UNIT I  
### MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY
9
NMOS and PMOS transistors – Threshold voltage – Body effect – Design equations– Second order effects – MOS models and small signal AC characteristics – Basic CMOS technology

## UNIT II  
### INVERTERS AND LOGIC GATES
9

## UNIT III  
### CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION
9
Resistance estimation – Capacitance estimation – Inductance – switching characteristics – transistor sizing – power dissipation and design margining – Charge sharing – Scaling

## UNIT IV  
### VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN
9

## UNIT V  
### VERILOG HARDWARE DESCRIPTION
9
Overview of digital design with Verilog HDL – Hierarchical modeling concepts– modules and port definitions – Gate level modeling– data flow modeling – behavioral modeling – Task & Functions – Test Bench

**Total: 45**

## TEXT BOOKS

## REFERENCES
UNIT I  BASIC SEMICONDUCTOR PHYSICS  
Quantum Mechanical Concepts – Carrier Concentration – Transport Equation – Bandgap – Mobility and Resistivity – Carrier Generation and Recombination – Avalanche Process – Noise Sources

UNIT II  BIPOLAR DEVICE MODELING  
Injection and Transport Model – Continuity Equation – Diode Small Signal and Large Signal (Change Control Model) – Transistor Models: Ebber – Molls and Gummel Port Model – Mextram model – SPICE modeling temperature and area effects

UNIT III  MOSFET MODELING  

UNIT IV  PARAMETER MEASUREMENT  

UNIT V  OPTOELECTRONIC DEVICE MODELING  
Static and Dynamic Models – Rate Equations – Numerical Technique – Equivalent Circuits – Modeling of LEDs – Laser Diode and Photo detectors

Total: 45

TEXT BOOKS

REFERENCES
1. Modeling of Sequential Digital system using VHDL.
3. Design and Implementation of ALU using FPGA.
4. Simulation of NMOS and CMOS circuits using SPICE.
5. Modeling of MOSFET using C.
8. Implementation of MAC Unit using FPGA.
UNIT I  MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES  

UNIT II  CIRCUIT CONFIGURATION FOR LINEAR IC  
Current sources – Analysis of difference amplifiers with active load using BJT and FET – Supply and temperature independent biasing techniques – Voltage references. Output stages: Emitter follower – Source follower and Push pull output stages

UNIT III  OPERATIONAL AMPLIFIERS  
Analysis of Operational Amplifiers circuit – Slew rate model and high frequency analysis – Frequency response of integrated circuits: Single stage and multistage amplifiers – Operational Amplifier noise

UNIT IV  ANALOG MULTIPLIER AND PLL  
Analysis of four quadrants and variable trans conductance multiplier – Voltage Controlled Oscillator – closed loop analysis of PLL – Monolithic PLL design in integrated circuits: Sources of noise – Noise models of Integrated – Circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise – Figure and Noise Temperature

UNIT V  ANALOG DESIGN WITH MOS TECHNOLOGY  

TEXT BOOKS

REFERENCES
UNIT I

UNIT II
Layout Compaction – Design rules – Problem formulation – Algorithms for Constraint Graph Compaction – Placement and partitioning – Circuit representation – Placement algorithms – Partitioning

UNIT III
Floor Planning concepts – Shape functions and Floorplan sizing – Types of Local Routing problems – Area routing – Channel routing – Global routing – Algorithms for Global Routing

UNIT IV
Simulation – Gate–level modeling and simulation – Switch–level modeling and simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis

UNIT V
High level Synthesis – Hardware models – Internal representation – Allocation assignment and scheduling – Simple Scheduling algorithm – Assignment problem – High level transformations

Total: 45

TEXT BOOKS

REFERENCES
UNIT I PRINCIPLES OF PARALLEL PROCESSING 9
Multiprocessors and Multicomputers – Multivector and SIMD Computers – PRAM and VLSI Models – Conditions of Parallelism – Program Partitioning and Scheduling – Program Flow mechanisms – Parallel Processing applications – Speed up Performance Law

UNIT II PROCESSOR AND MEMORY ORGANIZATION 9
Advanced Processor Technology – Superscalar and Vector Processors – Memory hierarchy technology – Virtual Memory technology – Cache Memory Organization – Shared Memory Organization

UNIT III PIPELINE AND PARALLEL ARCHITECTURE 9
Linear Pipeline Processors – Non Linear Pipeline processors – Instruction pipeline design – Arithmetic design – Superscalar and Super Pipeline design – Multiprocessor system interconnects – Message passing mechanisms

UNIT IV VECTOR– MULTITHREAD AND DATAFLOW ARCHITECTURE 9
Vector Processing principle – Multivector Multiprocessors – Compound Vector processing – Principles of Multithreading – Fine Grain Multicomputers – Scalable and Multithread Architectures – Dataflow and Hybrid Architectures

UNIT V SOFTWARE AND PARALLEL PROCESSING 9
Parallel programming models – Parallel languages and Compilers – Parallel programming environments – Synchronization and Multiprocessing modes – Message Passing program development – Mapping programs onto Multicomputers – Multiprocessor UNIX design goals – MACH/OS kernel architecture – OSF/1 architecture and applications

Total: 45

TEXT BOOK

REFERENCES
UNIT I EMBEDDED ARCHITECTURE

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM

UNIT III NETWORKS

UNIT IV REAL–TIME CHARACTERISTICS

UNIT V SYSTEM DESIGN TECHNIQUES

REFERENCES

Total: 45
1. Implementation of 8 Bit ALU in FPGA / CPLD.
2. Implementation of 4 bit sliced processor in FPGA / CPLD.
5. Implementation of model train controller using embedded microcontroller.
6. System design using PLL.
UNIT I

UNIT II
Test generation for Combinational Logic circuits – Testable Combinational Logic circuit design – Test generation for Sequential circuits – Design of testable Sequential circuits

UNIT III
Design for Testability – Ad hoc design – Generic scan based design – Classical scan based design – System level DFT approaches

UNIT IV
Built–In Self Test – Test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test algorithms – Test generation for Embedded RAMs

UNIT V
Logic Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self–checking design – System Level Diagnosis

TEXT BOOKS

REFERENCES
UNIT I  POWER DISSIPATION IN CMOS  
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design

UNIT II  POWER OPTIMIZATION  
Logical level power optimization – Circuit level low power design – Circuit techniques for reducing power consumption in Adders and Multipliers

UNIT III  DESIGN OF LOW POWER CMOS CIRCUITS  
Computer Arithmetic techniques for low power systems – Reducing power consumption in memories – Low power clock – Interconnect and layout design – Advanced techniques – Special techniques

UNIT IV  POWER ESTIMATION  
Power estimation techniques – Logic level power estimation – Simulation power analysis – Probabilistic power analysis

UNIT V  SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER  
Synthesis for low power – Behavioral level transforms – Software design for low power

Total: 45

TEXT BOOKS

REFERENCES
UNIT I FUNDAMENTAL TO DSP SYSTEMS
Introduction To DSP Systems – Typical DSP algorithms Iteration Bound – Data flow graph representations – Loop bound and Iteration bound – Longest path Matrix algorithm Pipelining and Parallel processing – Pipelining of FIR digital filters – Parallel processing – Pipelining and Parallel processing for low power

UNIT II RETIMING

UNIT III FAST CONVOLUTION

UNIT IV BIT–LEVEL ARITHMETIC ARCHITECTURES

UNIT V PROGRAMMING DIGITAL SIGNAL PROCESSORS

Total: 45
TEXT BOOKS

REFERENCES
UNIT I       MOS TRANSISTOR THEORY
Introduction to I.C Technology – Basic MOS transistors – Threshold Voltage – Body effect – Basic
D.C. Equations – Second Order effects – MOS models – Small signal A.C characteristics – The
complementary CMOS inverter – DC characteristics – Static Load MOS inverters – The Differential
Inverters – Transmission gate

UNIT II      CMOS PROCESSING TECHNOLOGY
Silicon semiconductor technology – Wafer processing – Oxidation – epitaxy – deposition – Ion
implantation – CMOS technology – nwell – pwell process – Silicon insulator – CMOS process
enhancement. Interconnect and circuit elements – Layout design rules – Latchup

UNIT III      CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION
Resistance estimation – Capacitance estimation – MOS capacitor characteristics – Device
capacitances – Diffusion capacitance – SPICE modeling of MOS capacitance – Routing capacitance
– Distributed RC effects – Inductance – Switching characteristics – Rise time – Fall time – Delay
time – Empirical delay models – Gate delays – CMOS gate transistor sizing – Power dissipation –
Scaling of MOS transistor dimensions

UNIT IV      CMOS CIRCUIT AND LOGIC DESIGN
CMOS Logic gate design – Fan in and fan out – Typical CMOS NAND and NOR delays –
Transistor sizing – CMOS logic structures – Complementary logic – BICMOS logic – Pseudo
nMOS logic – Dynamic CMOS logic – Clocked CMOS logic – Pass transistor logic – CMOS
domino logic – NP domino logic – Cascade voltage switch logic – Source follower pull up Logic
(SFPL) – Clocking strategies – I/O structures

UNIT V      CMOS SUBSYSTEM DESIGN
Data path operations – Addition/subtraction – Parity generators – Comparators – Zero/one detectors
– Binary Counters – ALUs – Multiplication – Array – Radix–n – Wallace Tree and Serial
Multiplication – Shifters – Memory elements – RWM Rom– Content Addressable Memory
Control: FSM – PLA Control Implementation

Total: 45

TEXT BOOKS
   Addison. Wesley, 2000

REFERENCES
   Edition
UNIT I  BASIC CMOS CIRCUIT TECHNIQUES– CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING


UNIT II  BASIC BICMOS CIRCUIT TECHNIQUES– CURRENT–MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING


UNIT III  SAMPLED–DATA ANALOG FILTERS– OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS


UNIT IV  DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS


UNIT V  STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER–AIDED DESIGN AND ANALOG AND MIXED ANALOG–DIGITAL LAYOUT


Total: 45
TEXT BOOKS

REFERENCES
UNIT I  RANDOM ACCESS MEMORY TECHNOLOGIES STATIC RANDOM ACCESS MEMORIES (SRAMs)
SRAM Cell Structures – MOS SRAM Architecture – MOS SRAM Cell and Peripheral Circuit Operation – Bipolar SRAM Technologies – Silicon On Insulator (SOI) Technology – Advanced SRAM Architectures and Technologies – Application Specific SRAMs

DYNAMIC RANDOM ACCESS MEMORIES (DRAMs)

UNIT II NONVOLATILE MEMORIES
Masked Read–Only Memories (ROMs) – High Density ROMs – Programmable Read –Only Memories (PROMs) – BipolarPROMs – CMOS PROMs – Erasable (UV) – Programmable Read–Only Memories (EPROMs) – Floating – Gate EPROM Cell–One Time Programmable (OTP) EPROM – Electrically Erasable PROMs (EEPROMs) – EEPROM Technology and Architecture – Nonvolatile SRAM – Flash Memories (EPROMs or EEPROM) – Advanced Flash Memory Architecture

UNIT III MEMORY FAULT MODELLING– TESTING– AND MEMORY DESIGN FORTESTABILITY AND FAULT TOLERANCE

UNIT IV SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS

UNIT V PACKAGING TECHNOLOGIES

Total: 45
TEXT BOOKS

REFERENCES
UNIT I CRYSTAL GROWTH – WAFER PREPARATION– EPITAXY AND OXIDATION


UNIT I LITHOGRAPHY AND RELATIVE PLASMA ETCHING


UNIT III DEPOSITION – DIFFUSION – ION IMPLEMENTATION AND METALISATION


UNIT IV PROCESS SIMULATION AND VLSI PROCESS INTEGRATION


UNIT V ANALYTICAL – ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES

Analytical Beams – Beams Specimen interactions – Chemical methods – Package types – Banking design consideration – VLSI Assembly technology – Package fabrication technology

Total: 45

TEXT BOOKS

REFERENCES
UNIT I FUNDAMENTAL TO VLSI TECHNOLOGY

UNIT II PLACEMENT USING TOP–DOWN APPROACH

UNIT III ROUTING USING TOP DOWN APPROACH

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT

UNIT V SINGLE LAYER ROUTING- CELL GENERATION AND COMPACATION

Total: 45
TEST BOOKS

REFERENCES
UNIT I
Introduction–GA Technology–Steady State Algorithm–Fitness Scaling–Inversion

UNIT II

UNIT III
Hybrid Genetic – Genetic Encoding–Local Improvement–WDFR–Comparison of Cas– Standard cell placement–GASP algorithm–Unified Algorithm

UNIT IV

UNIT V

Total: 45

TEXT BOOK

REFERENCES
UNIT I  MICROPROCESSOR ARCHITECTURE

UNIT II  HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM

UNIT III  HIGH PERFORMANCE RISC ARCHITECTURE: ARM
The ARM architecture – ARM Assembly Language Program – ARM Organization and implementation – The ARM instruction set – The Thumb instruction set – ARM CPU cores

UNIT IV  MOTOROLA 68HC11 MICROCONTROLLERS

UNIT V  PIC MICRO CONTROLLER
CPU architecture – Instruction set – Interrupts – Timers – I/O port expansion –I²C bus for peripheral chip access – A/D converter – UART

Total: 45

TEXT BOOKS

REFERENCES

Web links
www.ocw.nit.edu
www.arm.com
UNIT I  BASIC LEARNING ALGORITHM

UNIT II  RADIAL–BASIS FUNCTION NETWORKS AND SUPPORT VECTOR MACHINES: RADIAL BASIS FUNCTION NETWORKS:
Cover’s Theorem on the Separability of Patterns – Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks – Learning in Radial Basis Function Networks – Applications: XOR Problem – Image Classification

SUPPORT VECTOR MACHINES:

UNIT III  COMMITTEE MACHINES
Ensemble Averaging – Boosting – Associative Gaussian Mixture Model – Hierarchical Mixture of Experts Model (HME) – Model Selection using a Standard Decision Tree – A Priori and post priori Probabilities – Maximum Likelihood Estimation – Learning Strategies for the HME Model – EM Algorithm – Applications of EM Algorithm to HME Model

NEURODYNAMICS SYSTEMS:

UNIT IV  ATTRACTOR NEURAL NETWORKS
ADAPTIVE RESONANCE THEORY:

UNIT V SELF ORGANISING MAPS

PULSED NEURON MODELS: Spiking Neuron Model – Integrate–and–Fire Neurons – Conductance Based Models – Computing with Spiking Neurons

Total: 45

TEXT BOOKS

REFERENCES
UNIT I            FUNDAMENTAL TO ASICS- CMOS LOGIC AND ASIC LIBRARY DESIGN 
Types of ASICs – Design flow – CMOS transistors, CMOS Design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance– Logical effort –Library cell design – Library architecture

UNIT II           PROGRAMMABLE ASICS– PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS
Anti fuse – static RAM – EPROM and EEPROM technology – PREP benchmarks – Actel ACT – Xilinx LCA –Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock & Power inputs – Xilinx I/O blocks

UNIT III          PROGRAMMABLE ASIC INTERCONNECT– PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY

UNIT IV           LOGIC SYNTHESIS, SIMULATION AND TESTING
Verilog and logic synthesis –VHDL and logic synthesis – types of simulation –boundary scan test – fault simulation – automatic test pattern generation

UNIT V           ASIC CONSTRUCTION– FLOOR PLANNING– PLACEMENT AND ROUTING

Total: 45

TEXT BOOKS

REFERENCES
UNIT I  PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE  9
Statistical Distribution – Statistical Confidence and Hypothesis testing – Probability plotting
techniques – Weibull Extreme value Hazard – Binomial data – Analysis of load – strength
interference – Safety margin and loading roughness on reliability

UNIT II  RELIABILITY PREDICTION, MODELLING AND DESIGN  9
Statistical design of experiments and analysis of Variance Taguchi Method – Reliability prediction
– Reliability Modeling – Block diagram and Fault tree Analysis – Petri Nets – State space Analysis –
Monte Carlo simulation – Design analysis methods – Quality function deployment – Load strength
analysis – Failure modes – Effects and criticality analysis

UNIT III  ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY  9
Reliability of electronic components – Component types and failure mechanisms – Electronic system
reliability prediction – Reliability in electronic system design software errors – Software structure
and modularity – Fault tolerance – Software reliability – Prediction and measurement –
Hardware/software interfaces.

UNIT IV  RELIABILITY TESTING AND ANALYSIS  9
Test environments – Testing for reliability and durability – Failure reporting – Pareto analysis –
Accelerated Test Data Analysis – CUSUM charts – Exploratory Data analysis and Proportional

UNIT V  MANUFACTURE AND RELIABILITY MANAGEMENT  9
Control of Production Variability – Acceptance sampling – Quality control and Stress screening –
Production failure reporting preventive maintenance strategy – Maintenance schedules – Design for
Maintainability – Integrated Reliability programmes – Reliability and costs – Standard for reliability
– Quality and safety – specifying reliability – Organization for reliability

Total: 45

TEXT BOOKS
1. Patrick D.T. O’Connor, David Newton and Richard Bromley, “Practical Reliability
2. David J. Klinger, Yoshinao Nakada, Maria A. Menendez and Von Nostrand Reinhold, New

REFERENCES
UNIT I  EMI ENVIRONMENT
EMI/EMC concepts and definitions – Sources of EMI – conducted and radiated EMI – Transient EMI – Time domain Vs Frequency domain EMI – Units of measurement parameters – Emission and immunity concepts – ESD

UNIT II  EMI COUPLING PRINCIPLES
Conducted – Radiated and Transient Coupling – Common Impedance Ground Coupling – Radiated Common Mode and Ground Loop Coupling – Radiated Differential Mode Coupling – Near Field Cable to Cable Coupling – Power Mains and Power Supply coupling

UNIT III  EMI/EMC STANDARDS AND MEASUREMENTS

UNIT IV  EMI CONTROL TECHNIQUES

UNIT V  EMC DESIGN OF PCB

Total: 45

TEXT BOOKS

REFERENCES
UNIT I    MECHANICS OF SPEECH

UNIT II    TIME DOMAIN METHODS FOR SPEECH PROCESSING

UNIT III  FREQUENCY DOMAIN METHOD FOR SPEECH PROCESSING
Short Time Fourier analysis – Filter bank analysis – Formant extraction – Pitch Extraction – Analysis by Synthesis – Analysis synthesis systems – Phase vocoder – Channel Vocoder
HOMOMORPHIC SPEECH ANALYSIS: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoder

UNIT IV   LINEAR PREDICTIVE ANALYSIS OF SPEECH

UNIT V    APPLICATION OF SPEECH & AUDIO SIGNAL PROCESSING

Total: 45

TEXT BOOKS

REFERENCES
UNIT I  FUNDAMENTALS OF PROGRAMMABLE DSPs

UNIT II  TMS320C5X PROCESSOR
Architecture – Assembly language syntax – Addressing modes – Assembly language Instructions – Pipeline structure– Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals

UNIT III  TMS320C3X PROCESSOR
Architecture – Data formats – Addressing modes – Groups of Addressing Modes– Instruction sets – Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals – Generating and finding the sum of series – Convolution of two sequences – Filter design

UNIT IV  ADSP PROCESSORS
Architecture of ADSP–21XX and ADSP–210XX series of DSP processors – Addressing modes and assembly language instructions – Application programs – Filter design – FFT calculation

UNIT V  ADVANCED PROCESSORS
Architecture of TMS320C54X: Pipe line operation – Code Composer studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors

Total: 45

TEXT BOOK

REFERENCES
1. User guides, Texas Instrumentation Analog Devices, Motorola.

REFERENCES